CLAIM LISTING

1. (Original) A circuit for analyzing code coverage of firmware by test inputs, said circuit comprising:

an input for receiving an address from a code address bus;

a memory for storing recorded addresses from the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware; and

the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address.

2. (Previously Presented) The circuit of claim 1, further comprising:

an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to the memory.

3. (Previously Presented) The circuit of claim 2, further comprising:

a data multiplexer for making a second selection between an increment signal and a clear signal, and for providing the second selection to the memory.

4. (Original) The circuit of claim 3, wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address provided from the address counter is cleared.

5. (Original) A method for analyzing code coverage, said method comprising:

receiving an address from a code address bus, the address associated with an instruction in a system on chip; and

incrementing a memory location mapped to the address associated with the instruction.

6. (Previously Presented) The method of claim 5, further comprising:

making a first selection between the input and an address counter; and

providing the first selection to the memory.

7. (Previously Presented) The method of claim 6, further comprising:

making a second selection between an increment signal and a clear signal; and

providing the second selection to the memory.

8. (Original) The method of claim 7, wherein if the data the clear signal is selected, and the address counter is selected, then clearing a memory location mapped to an address provided from the address counter.

9. (Original) A circuit for analyzing code coverage of firmware by test inputs, said circuit comprising:

an input for receiving an address from a code address bus;

a memory operably connected to the input for storing recorded addresses from the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware; and

the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address.

10. (Previously Presented) The circuit of claim 9, further comprising:

an address multiplexer connected to the input and an address counter, the address multiplexer making a first

selection between the input and an address counter, and providing the first selection to the memory.

11. (Previously Presented) The circuit of claim 10, further comprising:

a data multiplexer connected to the memory, the data multiplexer making a second selection between an increment signal and a clear signal, and providing the second selection to the memory.

12. (Original) The circuit of claim 11, wherein if the data multiplexer selects the clear signal, and if the address multiplexer selects the address counter, then a memory location mapped to an address provided from the address counter is cleared.

13. (Previously Presented) The circuit of claim 1, wherein the contents of the memory location associated with the address received from the code address bus are incremented responsive to receipt of the address, thereby indicating a number of times the addressed has been received.

14. (New) The circuit of claim 2, wherein the multiplexer further comprises:

a first input that is directly connected to the input for receiving an address from a code address bus;

a second input that is directly connected to the address counter; and

an output that is directly connected to the memory.

15. (New) The circuit of claim 14, wherein multiplexer directly connects the first input to the output if the input for receiving an address from a code address bus is the first selection and directly connects the second input to the output if the address counter is the first selection.

16. (New) The circuit of claim 15, wherein the first selection is sometimes the input for receiving an address from a code address bus and is sometimes the address counter.